Engineering Electronic Properties of Graphene by Coupling with Si-Rich, Two-Dimensional Islands

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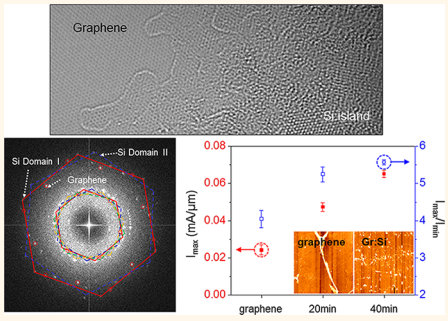
ABSTRACT Recent theoretical and experimental studies demonstrated that breaking of the sublattice symmetry in graphene produces an energy gap at the former Dirac point. We describe the synthesis of graphene sheets decorated with ultrathin, Si-rich two-dimensional (2D) islands (*i.e.*, Gr:Si sheets), in which the electronic property of graphene is modulated by coupling with the Si-islands. Analyses based on transmission electron microscopy, atomic force microscopy, and electron and optical spectroscopies confirmed that Si-islands with thicknesses of ~2 to 4 nm and a lateral size of several tens of nm were bonded to graphene *via* van der Waals interactions. Field-effect transistors (FETs) based on Gr:Si sheets exhibited enhanced transconductance and maximum-to-minimum current level compared to bare-graphene FETs, and their magnitudes gradually increased with increasing coverage of Si layers on the graphene. The temperature dependent current—voltage measurements of the Gr:Si sheet showed approximately a 2-fold increase in the resistance by decreasing the temperature from 250 to 10 K, which confirmed the opening of the substantial bandgap (~2.5—3.2 meV) in graphene by coupling with Si islands.



KEYWORDS: graphene · silicon islands · van der Waals growth · bandgap engineering · sublattice asymmetry

The potential of atomically thin graphene layers with excellent electrical[1,2] and thermal conduction and mechanical strength[4] has motivated research toward future electronics.[5] As graphene is a one-atom thick planar sheet of carbon atoms in a honeycomb crystal lattice, three electrons from each carbon atom involve strong sp^2 hybrid bonds with their neighbors that form a σ state, while the fourth electron is delocalized and develops into a π state. The extremely high mobility of graphene, with reported values in excess of 15 000 $cm^2\ V^{-1}\ s^{-1}$ at room temperature, is associated with its linear electronic band dispersion relation near the Dirac points such that the carriers (electrons and holes associated with the π bands) behave like massless Dirac fermions.[6,7] On the other hand, the π bonding and π^* antibonding states of graphene are degenerate at the Dirac points, and, thus, graphene exhibits a semimetallic behavior or zero-bandgap nature that limits the practical application in electronic devices.

Several routes have been designed and implemented to engineer the bandgap in graphene without degrading its intrinsic carrier mobilities.[8−11] One route is the use of narrow graphene nanoribbons,[8,9] nanomeshes,[10] or quantum dots,[11] where lateral constriction of the charge carriers causes a bandgap. However, this approach requires patterning of graphene with a width much smaller than ~10 nm to achieve a substantial bandgap, and the electronic structure is quite sensitive to the edge atomic configuration and size. Hybridized structures consisting of a graphene matrix with a dispersed phase of wider gap 2D layer-structured materials, such as hexagonal boron nitride (h-BN) sheets[12] or hydrogenated graphene[13] (i.e., graphane), were also introduced to induce electron confinement. However, electron scattering at the domain boundaries significantly degraded the electronic properties. As the degeneration of the π and π^* bands at the Dirac points is associated with the

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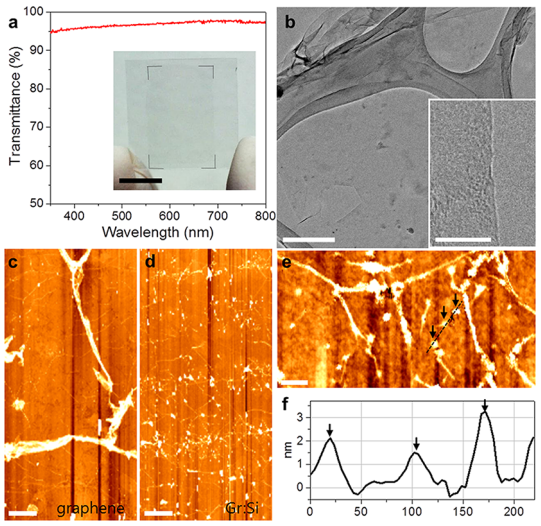

Figure 1. (a) Optical transmittance spectrum of the Gr:Si sheet. Inset: photograph of the Gr:Si sheet transferred to a glass substrate. Scale bar, 1 cm. (b) Low-magnification TEM image of the free-standing Gr:Si fragment deposited on a holey carbon grid. Scale bar, 200 nm. Inset: TEM image of the edge of the monolayer Gr:Si sheet. Scale bar, 5 nm. (c, d) Comparison of AFM surface topographies of graphene (c) and Gr:Si (d) sheets. Scale bars, 1 μm. (e) Enlarged AFM image of a selective area in panel d. Scale bar, 100 nm. (f) Height profile along the black dotted line.

lattice symmetry of carbon atoms in a honeycomb crystal lattice,[14] the breaking of the sublattice symmetry is an alternative to open its bandgap.[15] One example is the substrate-induced bandgap opening of graphene epitaxially grown on specific substrates,[16] such as silicon carbide (SiC); however, their existence and origin are still under debate. Moreover, the use of specific substrates imposes severe restrictions on the application of graphene.

In this study, the engineering bandgap in graphene was investigated by introducing Si-rich, two-dimensional (2D) islands dispersed on the graphene sheet. In the graphene sheet decorated with Si-islands (Gr:Si sheet), the interaction between graphene and the islands breaks the sublattice symmetry and thereby opens the bandgap.

RESULTS AND DISCUSSION

Synthesis and Transfer of Gr:Si Sheets. As a first step of this study, single-layer graphene sheets were grown on copper foils by the custom-built CVD at 1000 °C for 30 min. After transferring the graphene to Si/SiO_2 substrate, a vapor transport route using Si lumps as source materials was used to deposit Si-islands on graphene. The deposition process was performed in a flowing H_2/Ar atmosphere at 1000 °C for 20−60 min (see Methods section and Supporting Information Figure S1). Because of the strong sp^2-hybridized C−C bond in graphene, displacement of C by Si hardly occurred. Instead, physisorbed Si adatoms formed very thin Si-islands bonded to the graphene *via* van der Waals interactions. Even after the Si island deposition, graphene sheets sustained their 2D layered form such that they were readily separated from the growth substrates and transferred to other substrates for characterization and device fabrication (see the Methods section and Supporting Information, Figure S1). A continuous form of a large area ($\sim 1 \times 2$ cm^2) Gr:Si sheet transferred to a glass substrate is shown in the inset of Figure 1a. Additional optical transmittance measurements reveal that the sample was highly transparent with an average transmission of ~97% in the visible spectral range (Figure 1a), which is comparable to monolayer graphene.[17,18]

Figure 1b shows the low-magnification transmission electron microscopy (TEM) image of a free-standing membrane with a lateral size of several micrometers. The central region of the sample reveals the characteristic feature of atomically thin 2D layered structures, whereas the edges of the free-standing sheets tended to fold back enabling the layer number to be measured. TEM examination confirmed the formation of a monolayer or ~2−3 layer sheets (inset, Figure 1b). In addition, atomic force microscopy (AFM) surface topography of the Gr:Si sheet reveals a continuous sheet with the exception of a few wrinkles, which is similar to that of the CVD-grown graphene sheet (Figure 1c,d). Meanwhile, white bumps were distributed relatively uniformly on graphene (Figure 1d,e). These bumps correspond to Si islands, and their height and width were estimated as ~1−3 nm and ~20−50 nm, respectively (Figure 1f).

Structural and Composition Analyses. Further structural characterization was performed using a low-acceleration voltage aberration-corrected TEM analysis. As shown in the low-magnification phase contrast image (Figure 2a), uniform distribution of the islands on the graphene sheet was visualized by dark contrast features, which is analogous to the AFM results. The magnified TEM image at the edge of the islands reveal that the atomic structures of the islands are distinctly different from that of graphene (Figure 2b). A lattice-resolved image obtained by zooming in on one of the graphene regions illustrates that significant areas of the graphene regions appear clean with near-perfect atomic arrangements in a honeycomb crystal lattice, except for the carbon adsorbates near the edge of the image (Figure 2c). In Si-rich island regions, polycrystalline structures, consisting of nanocrystalline domains, are clearly visible (Figure 2d). Each domain exhibits hexagonal lattice fringes with an adjacent lattice spacing of 0.19 nm, which is consistent with the *d*-spacing of the Si $(0\bar{2}2)$ planes.[19] The corresponding fast Fourier transformation (FFT) image transformed from Figure 2e reveals the existence of several sets of hexagonal diffraction patterns with identical size and configuration. Additionally, each set is identical to the Si [111] zone axis patterns, confirming that the preferred crystal orientation perpendicular to the graphene surface is [111]. Several color-shade domains in Figure 2d correspond to the diffraction patterns in Figure 2e, which

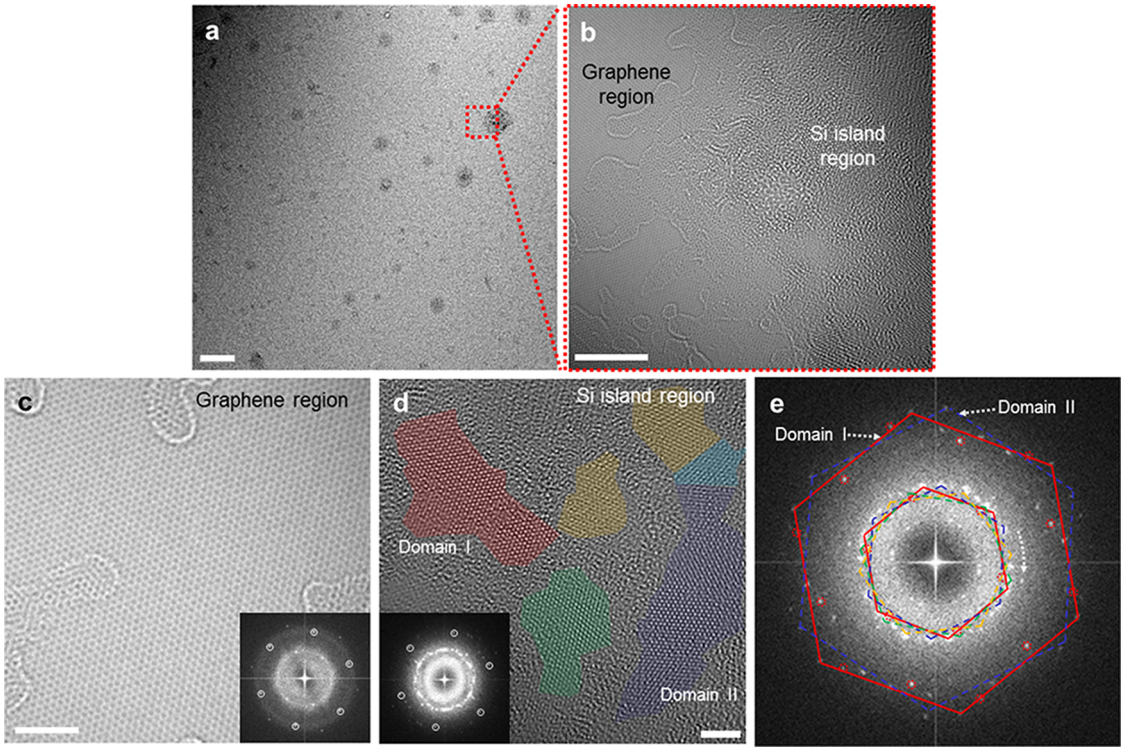

Figure 2. Low-acceleration voltage aberration-corrected TEM images of the Gr:Si sheet. (a) Low-magnification phase contrast image of the Gr:Si sheet. Scale bar, 50 nm. (b) Enlarged TEM image at the edge of the island. Scale bar, 5 nm. (c, d) High-resolution TEM images of bare graphene (c) and Si-island (d) regions. Scale bars, 2 nm. Insets of (c, d): FFT images of panels c and d. (e) A zoom-in FFT image of inset of panel d, where the colored hexagonal lines and spots correspond to colored nanocrystal domains in panel d.

illustrates that these domains have one common crystal plane parallel to the graphene but at random in-plane orientations. These observations are slightly different from the van der Waals epitaxy of InAs[20] and Bi_2Se_3[21] on graphite or exfoliated graphene, and can be attributed to a large lattice mismatch, surface roughness, and carbon absorbates on graphene surfaces. An additional set of hexagonal spots (white circles in the insets of Figure 2d) also appeared, and the size and orientation are identical to that in the pure graphene region (insets of Figure 2c). This result indicates that the graphene underneath the Si-islands remains as an sp^2 honeycomb lattice structure, even after the Si island formation.

The changes in the atomic composition and structure depending on the Si island formation were further investigated by electron energy loss spectroscopy (EELS) (Figure 3a). Both bare-graphene and Si island regions exhibit characteristic C K-shell edge peaks, verifying the distinctive sp^2 feature of the C elements.[22,23] Because of very strong sp^2 hybrid bonds of carbon atoms in the graphene planes, the growth of Si 2D islands on the graphene occurs by van der Waals interaction, rather than covalent bonds.[24] Apart from the K-shell ionization edge of C, the characteristic edge onset at ~102 eV appears in the EELS spectrum of the Gr:Si sheet, corresponding to the Si $L_{3,2}$ edge representing the excitation of Si $2p^{3/2}$ and $2p^{1/2}$ electrons.[25] This Si L edge feature, which is not

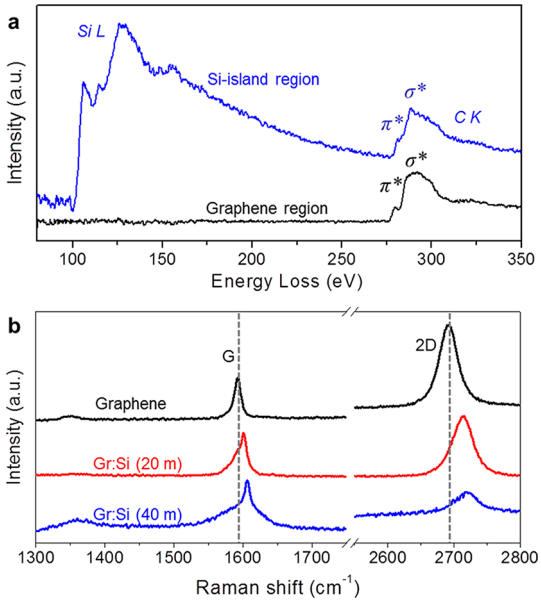

Figure 3. (a) EELS spectra of Gr:Si sheet achieved at the bare-graphene (black) and Si island (blue) regions. (b) Raman spectra before (black) and after the Si decoration reactions for 20 min (~8 atom % of Si, red) and 40 min (~10 atom % of Si, blue).

observed in graphene, illustrates the existence of Si atoms on graphene. However, the current Si $L_{3,2}$ edge feature, starting at 102 eV and reaching the first maximum at 106 eV, is different from Si crystal that is

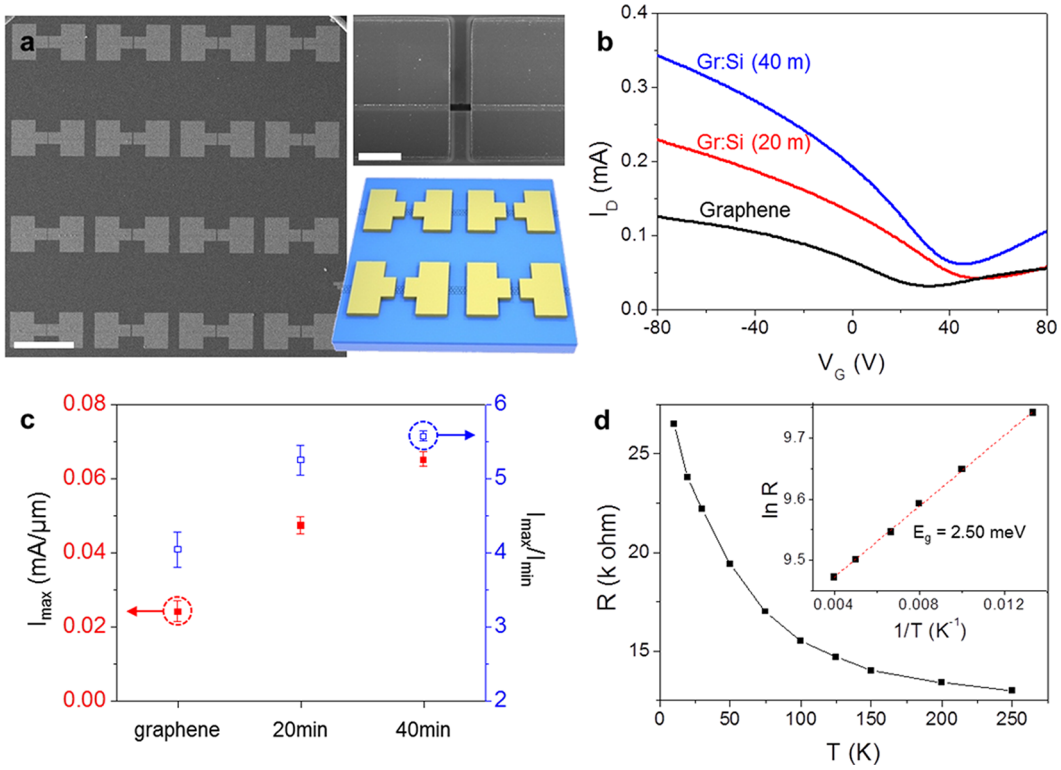

Figure 4. Field-effect transistor characteristics of Gr:Si sheets. (a) SEM images and schematic illustration of the Gr:Si FET array. Scale bars: 500 μm, 30 μm. (b) I_D-V_G characteristic curves at a V_D of 1 V recorded for typical FETs with a graphene channel (black) and Gr:Si channels synthesized *via* Si reactions for 20 min (~8 atom % Si, red) and 40 min (~10 atom % Si, blue). (c) Statistical analyses of I_{max}/I_{min} and I_{max} as a function of the Si decoration reaction time. (d) Temperature-dependent electrical transport measurement result of Gr:Si (~8 atom % of Si) FET.

characterized by a main peak starting near 100 eV with a first maximum at ~101−102 eV. The shift of the edge spectrum may be associated with the oxidation and/or carbidation states of Si.[26] As the crystalline Si structure was confirmed in the TEM image and absence of O K edge peak in EELS spectrum (see Supporting Information, Figure S2), the Si islands consisted of extremely thin Si domains whose surface and boundary can be oxidized/carbidized easily, resulting in the change in the absorption spectrum.

Figure 3b displays the evolution of the Raman spectra following the reaction of Si with graphene sheets. Unique features include the increase in the disorder-induced D bands (~1350−1355 cm^{-1}), broad background signal and a decrease in 2D bands, which illustrates the gradual change from the original graphene characteristics. In addition, both the G and 2D bands of the Gr:Si sheets shift toward higher frequencies in the graphene spectrum, from 1592 to 1601 cm^{-1} and 2692 to 2,713 cm^{-1}, respectively.[27] The shift in the G band (9 cm^{-1}) is much greater than that of the 2D band (21 cm^{-1}) and different mechanisms can be introduced to explain these shifts. The signal shift in the G band accompanying Si decoration is explained by local electron/hole doping in carbon-based materials.[28] Even though local doping can affect the 2D band of the carbon material, a 2D band shift of 21 cm^{-1} is too large to occur with such doping.[29] Instead, the strain effect can explain the 2D band shift of Gr:Si structures, as similar phenomena have been observed in epitaxial graphene grown on a SiC substrate[29] and a Be_2Se_3 nanoplate[21] on graphene.

Electrical Properties of the Gr:Si Sheets. To investigate the electrical properties of the Gr:Si sheets, back-gate field-effect transistors (FETs) were fabricated on a degenerately doped n^+-Si wafer with a 300-nm thick oxide layer, following the procedure described in the Supporting Information. Specifically, the capability of large-area transfer and patterning of arbitrary shapes with nanometer or micrometer features enables the creation of large-scale FET arrays (Figure 4a). Optical and SEM images illustrate that the FETs consisted of Gr:Si channels with a width of 5 μm and source-drain electrode pair with a gap of 10 μm. Figure 4b compares the source-drain current (I_d) *versus* back-gate voltage (V_g) characteristic curves for graphene and Gr:Si sheets, which illustrates several interesting points. First, compared with the graphene-FET exhibiting a minimal conductance at a finite gate voltage (corresponding to the Dirac point) at ~20 V, Gr:Si FETs exhibit shifts in their Dirac points up to 40−60 V, indicating that they operate more as p-channel transistors. Second, the maximum current (I_{max}) (or current at V_g of −80 V) increases from 0.125 mA to 0.229 mA for the Gr:Si FET with the Si reactions for 20 min (~8 atom % Si) and to

0.342 mA for 40 min (~10 atom % Si) with respect to the graphene FET. Third, following the I_{max} increase, the maximum-to-minimum current ratio (I_{max}/I_{min}) also gradually increased from 4.0 to 5.2 and 5.5 with increasing Si-concentration. The enhanced I_{max}/I_{min} ratio and the Dirac point shifts strongly suggest the gradual conversion of Gr:Si sheet characteristics from semimetallic to semiconducting. Moreover, statistical analyses of 30 devices reveal similar behaviors. As shown in Figure 4c, the I_{max} increased by a factor of ~3 and the I_{max}/I_{min} increased from ~4 to 5.5, after the Si reaction for 40 min. From the slope of the I_d-V_g curve, a peak transconductance, $G_M = dI_d/dV_g$, of Gr:Si FETs was ~3 μS, corresponding to a calculated hole mobility of $\mu = \sim 780$ cm^2/(V·s). This value is larger than that of pristine-graphene FET (~360 cm^2/(V·s)) and also analogous to the previously reported values of graphene FET (~1,000 cm^2/(V·s)),[30] illustrating that alloy disorder scattering is not severe in this sample.[12] In addition, we have investigated change in the I_D-V_G characteristics before and after Si island formation, using a different batch of graphene sheets than those used for the data in Figure 4b,c, and their results are displayed in Supporting Information, Figure S3. Although the electrical properties of graphene FETs in Figure S3 are different from those in Figure 4b,c, the effect of Si island deposition on the I_{max} and I_{max}/I_{min} ratio are essentially same.

Moreover, temperature-dependent electrical transport measurements on Gr:Si sheets with the Si reactions for 20 min (~8 atom % Si) show the resistance increases by decreasing temperature from 250 to 10 K (Figure 4d), which is different from that of graphene and corresponds to a typical semiconducting behavior. The electrical resistance of the Gr:Si sheet as a function of temperature is given as Arrhenius plots in the inset of Figure 4d. The linear relationship between the logarithm of resistance and inverse of temperature confirmed that the Arrhenius law was satisfied, with which the bandgap energy was calculated as 2.5 meV. Moreover, the measured bandgap of Gr:Si sheets increased with increasing Si coverage, from 2.5 meV for 8 atom % Si to 3.2 meV for 10 atom % Si (Supporting Information, Figure S4). We believe that the bandgap generation originated from the breaking of the A,B sublattice symmetry of graphene caused by coupling with the ultrathin Si-islands. Similar phenomena have been observed in bi- or trilayer graphene[31,32] and monolayer graphene grown epitaxially on the SiC substrate,[16] where the interactions between different layers can cause the graphene to lose the 6-fold rotational symmetry near the Dirac point, breaking the A,B sublattice equivalence.[11,16,32] However, the bandgap energy of 3.2 meV is too small in comparison with those of epitaxial graphene grown on a SiC substrate (~250 meV), and can be attributed to the small coverage of Si islands (less than 10%). In this case, modulation of the band structure occurs only in localized regions of graphene just below the Si islands. We therefore expect that the substantial bandgap created by coupling with Si-islands should be much greater than the measured values (of 3.2 meV), and thus the bandgap energy of the Gr:Si can be further enlarged by increasing the Si coverage.

The bandgap creation is associated with the improved I_{max}/I_{min} ratio in the Gr:Si FETs; however, its magnitude is ten times smaller than the thermal energy at room temperature (26 meV) such that the Gr:Si FETs could not be fully turned off. However, the other changes observed in the Gr:Si FETs, that is, the enhanced current level, transconductance, and field-effect mobility, cannot be solely understood by the modulation of the bandgap. We believe that the Si decoration process resulted in the recovery of defects in graphene,[33] such as Stone-Wales defects,[34] vacancies of carbon atoms, and line defects at the grain boundary that deteriorate the charge carrier transport in graphene. Recent theoretical calculations based on a density functional theory predicted the substitutionally doped Si atoms in graphene do not significantly disturb the quantum conductance of the pristine graphene, which is distinctly different from other elements (such as B, N, P, and S) that cause defect scattering in graphene.[35] Accordingly, defect reconstruction accompanying Si incorporation could be another possible scenario, where Si atoms occupying the vacancy sites in graphene can lead to an injection of charge carriers into the electrical system of graphene without providing any significant defect scattering sites. On the other hand, Si-islands on graphene can break not only the A,B sublattice symmetry but also the electron–hole symmetry in pristine graphene. The resulting electron–hole asymmetry caused the self-doping effect that is associated with the Dirac point shift (downshift of the Fermi level) in the graphene near the Si-islands,[36] leading to a current level increase in the Gr:Si FETs. This self-doping effect created a synergy with a bandgap opening to enhance the transconductance and motility of the Gr:Si FETs.

CONCLUSIONS

Large-area synthesis of graphene sheets decollated with Si-islands was performed. Analyses based on AFM and aberration-corrected TEM revealed that a few nm thick 2D Si-islands were tightly bonded to graphene by van der Waals interactions. Even after Si island deposition, the graphene layer maintained its sp^2 honeycomb structures, as confirmed by EELS and Raman spectroscopy. Importantly, electrical transport measurements showed that the electronic properties of graphene can be modulated by coupling with the Si-islands, leading to a bandgap opening and an improvement of the transistor characteristics, including the current level, transconductance, and mobility of the Gr:Si FETs compared to

the pristine graphene-FETs. This new Gr:Si structure provides an opportunity to control the electronic band structure in graphene-integrated systems and an intriguing possibility of flexible, wearable, and invisible electronics.

METHODS

Synthesis of Gr:Si Nanosheets. Initially, a large, mostly single layer graphene specimen was synthesized on copper foils by chemical vapor deposition (CVD) and then mounted onto a Si substrate with a 300-nm-thick SiO_2 layer. A detailed description of the CVD synthesis and transfer of graphene can be found elsewhere.[18,37] Immediately following the transfer, the graphene films on SiO_2/Si substrates were loaded into the CVD tube reactor (1 in. diameter quartz tube) again, where tiny fragments of single crystal Si in an alumina crucible were placed at a distance 3−4 cm upstream from the growth substrates. The decoration reaction of graphene into Gr:Si sheets was carried out at 1000 °C for 20−60 min, while the pressure was maintained in the range of 50−200 Torr under the continuous supply of a 30−50 SCCM H_2/Ar gas mixture (10% H_2 in Ar).

Transfer of the Gr:Si Sheets to Arbitrary Substrates. After synthesis of the Gr:Si sheet, it was separated from the SiO_2/Si substrate by selective etching of the SiO_2 layer. Typically, the film was initially coated with a poly(methyl methacrylate) (PMMA C9) protecting layer, and then dipped in 1:10 HF-solution. After rinsing the separated Gr:Si/PMMA film in deionized (DI) water, it was transferred to a target substrate for analysis and characterization. The PMMA protecting layer was typically removed with acetone.

TEM and EELS Measurements. The approach that utilizes direct transfer of the Gr:Si/PMMA film to the TEM grid and subsequent removal of the PMMA with acetone cannot fully remove residual PMMA on the surface, which significantly affects the high-resolution TEM analysis of the sheet. To minimize the amount of residual PMMA, we slightly modified the transfer method for TEM measurement. After preparing the Gr:Si/PMMA film by following the procedure described in the previous section, it was transferred to another copper foil. Subsequently, the PMMA support was completely removed with acetone. Finally, the Gr:Si sheet was detached from the copper foil with diluted ammonium persulfate acid and then transferred to the TEM grid. We noted that the freestanding Gr:Si sheet with no supporting layer was easily cracked and torn, but its fragments several micrometers to millimeters in lateral size could be easily found in the grid. High-resolution TEM, electron diffraction, and EELS analyses were carried out with an aberration-corrected TEM which operated at 80 keV.

Transistor Fabrication and Electrical Characterization. The Gr:Si sheet was transferred onto a heavily doped n^+-Si wafer with a 300-nm-thick oxide layer to fabricate the back-gate field-effect transistor. Channels of the Gr:Si transistor with a 5 μm width were patterned by conventional photolithography, followed by oxygen plasma etching at 50 W for 1 min. Subsequently, the second photolithography process and thermal evaporation of Ti/Au (10 nm/50 nm) were performed to define the source−drain electrodes. To reduce the contact resistance, the SiC-sheet field-effect transistor was thermally annealed at 380 °C for 90 s in the vacuum. Electrical measurements were conducted using a probe station with a semiconductor parameter analyzer (model HP4145A).

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: Additional figures as described in the text. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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